VLSI Architectures for Low-Energy Machine Learning Systems

Prof. Keshab K. Parhi

Dept. of Electrical & Computer Engineering

University of Minnesota, Minneapolis

Email: parhi@umn.edu

<http://ece.umn.edu/~parhi>

Abstract: Reducing energy consumption of machine learning systems requires selection of discriminative features, selection of electrodes in multi-channel systems, and approximate computing based architectures for computing features and classifiers. In this talk, I will describe a new feature selection method referred as *minimum-uncertainty sample elimination* (MUSE) that can lead to selection of fewer features, and an incremental-precision based feature computation followed by multi-level classification. The proposed approach makes use of approximate computing and leads to an overall reduction in energy consumption.

Bio:

Keshab K. Parhi received the B.Tech. degree from the Indian Institute of Technology (IIT), Kharagpur, in 1982, the M.S.E.E. degree from the University of Pennsylvania, Philadelphia, in 1984, and the Ph.D. degree from the University of California, Berkeley, in 1988. He has been with the University of Minnesota, Minneapolis, since 1988, where he is currently Distinguished McKnight University Professor and Edgar F. Johnson Professor in the Department of Electrical and Computer Engineering. He has published over 600 papers, is the inventor of 29 patents, and has authored the textbook *VLSI Digital Signal Processing Systems* (Wiley, 1999) and coedited the reference book *Digital Signal Processing for Multimedia Systems* (Marcel Dekker, 1999). His current research addresses VLSI architecture design of signal processing systems, hardware security, data-driven neuroscience and molecular computing. https://mail.google.com/mail/u/0/images/cleardot.gifDr. Parhi is the recipient of numerous awards including the 2017 Mac Van Valkenburg award and the 2012 Charles A. Desoer Technical Achievement award from the IEEE Circuits and Systems Society, the 2004 F. E. Terman award from the American Society of Engineering Education, the 2003 IEEE Kiyo Tomiyasu Technical Field Award, the 2001 IEEE W. R. G. Baker prize paper award, and a Golden Jubilee medal from the IEEE Circuits and Systems Society in 2000. He was elected a Fellow of IEEE in 1996 and a Fellow of the AAAS in 2017.